REMARKS/ARGUMENTS

The rejections under 35 USC 112

The Examiner rejects Claims 1, 10, and 17 under 35 USC 112 first paragraph, the Examiner alleging that the application fails to comply with the written description requirement. The Examiner asserts that claims contain subject matter which was not described in the specification in such a way as to be reasonably conveyed to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

The Examiner starts off by asserting that a new claim limitation not found in the original description is "silicon substrate". The Examiner's attention is respectfully directed to element 30 shown in a number of the figures of this application, including Figures 10a and 10b. Please consider Figure 10a wherein the notation "Si substrate" is found in the region of the depicted device identified by the numeral 30. In the specification, the term "wafer board" is sometimes used with respect to numeral 30. It is believed that it is reasonably well-known in this art that the term "silicon wafer board" is one way of describing a "silicon substrate". And given the fact that the term "Si substrate" is used on the drawings themselves, the connection between the silicon wafer board and the silicon substrate is more than amply made clear in the patent application as filed.

The Examiner's assertion that the limitation "silicon substrate" is not set forth in the patent application, as filed, is, with all due respect, without merit.

The next assertion by the Examiner is that "the gain element having a body of material different than said integration platform" is not disclosed in the patent application as filed. The aforementioned reference numeral 30 is also used with respect to the described "integration platform". Thus, the integration platform into the

preferred embodiments disclosed in this patent application, are preferably implemented as a silicon substrate or a silicon wafer board. The gain element is identified by the reference numeral 20 in the application as filed. The application as filed also indicates that there are a number of gain elements 20 well known in the art and an exemplary one is shown in Figure 6 which depicts a GaInAsP/InP semiconductor optical amplifier as a possible gain element. Please see paragraph 0039 of the application as filed. It is believed that those skilled in the art realize that a GaInAsP/InP semiconductor optical amplifier 23 is a gain element which has a body of material different than that of a silicon integration platform. The Examiner's assertions to the contrary are not meritorious.

The Examiner goes on to assert that there is no disclosure of a "silica wave guide" in the application as filed. That is not correct. Note the reference to "silica waveguides" in paragraphs 0014, 0030, 0041, 0044, etc. of the application as published or the reference to "silica waveguide" in Figure 10a. The Examiner's assertion that there is no disclosure of "a silica waveguide" in the application as filed is without merit and should be withdrawn as having been made improperly.

The next assertion by the Examiner is that the limitation "tunable resonator" having a body of material different than said silica waveguide" is not disclosed in the application as filed. That is not correct. It has already been indicated that one possible embodiment of the gain element is the aforementioned GaInAsP/InP semiconductor optical amplifier 23. The material of that amplifier is obviously different than the silica waveguide. An assertion made by the Examiner is incorrect and should be withdrawn.

Next, the Examiner asserts that the limitation "fixed grading inside integration platform" is not disclosed in the application as filed. The Applicant respectfully disagrees. The Examiner's attention is directed to Figure 5 of the application as filed which shows, at reference numeral 40, a fixed optical grading. As shown in Figure 5 and as set forth in original Claim 2, the fixed optical grading is preferably integrated

with the integration platform. It is submitted that the limitation is more than adequately described in the application as filed.

The next assertion by the Examiner is that the limitation "UV-induced sample grading" is not disclosed in the application as filed. This is also not correct. Please see, for example, paragraph 0054 of the application as published.

Next the Examiner asserts that "sampled grading fabricated on or over a silica waveguide" is not disclosed in the application as filed. Please see Figure 5 of the application as filed showing one view of the juxtaposition of a silicon waveguide 102 and grading 40. It is noted, in this connection, that paragraph 0054 of the application as filed indicates that in one embodiment the grading 40 is fabricated in waveguide 102. Nevertheless, claim 17 has been amended to use the "in" terminology also found in paragraph 0054 of the application as filed.

The rejections of Claims 1, 10 and 17 and their dependent claims under 35 USC 112, first paragraph, is without merit and should be withdrawn.

The Examiner rejects Claims 25 and 26 under 35 USC 112, first paragraph, as failing to comply with the written description requirement. This grounds for rejection is respectfully traversed.

The Examiner begins by asserting that the application, as filed, does not teach "microresonator has a body comprising GaInAsP/InP" material. The Applicant disagrees. A tunable resonator is described in the application and depicted in the drawings with reference to reference numeral 50 and more particularly with reference to numeral 50a. In paragraph 0042 of the application as published, microdisk 50a is described as a "GaInAsP/InP microdisk 50a". It is believed that a person of ordinary skill in the art would appreciate that the body of the microdisk 50a if it is a "GaInAsP/InP microdisk", then it would have a body ofGaInAsp/InP. Would a person reading this application reasonably understand that the body of the microdisk was something other than GaInAsP/InP if it were a "GaInAsP/InP microdisk 50a"?

The Examiner next asserts that "microresonator from III-V semiconductor material" is not disclosed in the application as filed. It is submitted that it is well-known that a GaInAsP/InP microresonator comprises III-V semiconductor material. And in paragraph 0041 of the application as published, there is a discussion of how the tunable resonator 50 is coupled to the waveguides 101, 102. The discussion is in terms of III-V materials and a silicon-based device and moreover it is indicated that the microresonator 50 "may be fabricated from a semiconductor material such as GaAs or InP" given the fact that a number of Group III-V materials are described in the application with reference to the microresonator 50, and the term III-V has been used specifically in terms of bonding it to the waveguides, it is submitted that there is more than ample disclosure in the patent application for the quoted expression.

The Examiner indicates Claims 24-26 are patentable over the prior art and would be allowed if rewritten to overcome a 35 USC 112, second paragraph, rejection. It is assumed that the Examiner is referring to the informality mentioned in paragraph one of the Official Action since a 35 USC 112, second paragraph, rejection was not found. It is believed that the rejections of Claims 25 and 26 under 35 USC 112, first paragraph, have been overcome and that the matter raised by the Examiner in paragraph one of the Official Action has also been attended to.

The remaining claims are rejected on prior art grounds.

The prior art based rejections

The Examiner rejects claim 17 under 35 USC 103 as being unpatentable over Frick (US 2004/01206738) in view of Painter (US 2002/0122615). This grounds for rejection is respectfully traversed.

The Examiner asserts that it would be obvious to modify Frick's waveguides to use lateral confinement as taught by Painter. The Examiner makes an assumption that Frick's waveguides have a lateral confinement issue which needs to be addressed using

the technology discussed in Painter. What is that assumption based upon? Or to put it more bluntly, if Frick's waveguides aren't broken, what is the motivation to fix them? Also note that Painter's multi-layer reflector stacks occur along the sides of his waveguide.

In any event claim 17 has been clarified to indicate that grating is "fabricated in a silica waveguide for reflection back to said gain element" which is quite unlike the function of Painter's gratings.

Claims 1, 3-9, 17, 19, 20 and 22 were rejected as being unpatentable over Orenstein (US 6,940,878) in view of Soref (US 6,195,1875) and Bilodeau (IEEE Photonics Technology Letters). This grounds for rejection is respectfully traversed.

Orenstein teaches a tunable laser using a microring resonator whereas Soref teaches a WDM (Wavelength Division Multiplexer) Cross-Connect Switch.

The Examiner proposes to modify Orenstein based on Soref "to allow cross connect." It is to be noted that Orenstein makes a big deal about his process allowing his laser to be built "monolithically". See the first paragraph after the subtitle "Summary of the Invention". Note also the discussion at column 2, lines 33-37 about the laser being a "semiconductor laser" and the desire for "an active region located within at least a segment of one of the waveguides".

So after a person reads with stuff in Orenstein, why are they supposed to be motivated (i) to use resonators of a material different than the resonators or (ii) silica waveguides? The Examine states that the motivation to disregard this clear and unambiguous teaching of Orenstein is "to allow cross connect". Why does Orenstein's laser need cross connect? And even assuming it did need cross connect (for some undisclosed reason), would not a person skilled in the art be motivated to add cross connect monolithically using a semiconductor laser with an active region located within at least a segment of one of the waveguides as opposed to going against the clear teachings of Orenstein?

The same issue arises with the citation of Bilodeau.

The Examiner has not made a proper prima facie case for obviousness based on Orenstein and Soref much less based on Orenstein and Soref and Bilodeau.

The Examiner's indication of allowable subject matter in terms of claims 24-26, but it is believed that all of the claims in this application patentably define over the prior art of record.

Reconsideration is respectfully requested.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Office with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

13 November 2006
(Date of Deposit)

Mary Ngo
(Name of Person Depositing)

(Signature)

13 November 2006
(Date)

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